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Wired for Resilience: Transatlantic Approaches to Semiconductor Supply Chain Security

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Ministry of Foreign Affairs and International Cooperation

ABSTRACT

Semiconductors, the bedrock of modern economies, have vaulted from niche concern to the centre stage of economic security policy amid the intensifying United States–China technology rivalry. Caught in the middle is the global semiconductor ecosystem, intricately interdependent and now geopolitically exposed. The central policy question is how can the United States and its allies de-risk and diversify without succumbing to techno-nationalist overreach? Securing semiconductor resilience is not a zero-sum nationalist arms race. It is a positive-sum coordination challenge. The United States and Europe must act not just in parallel but in concert – aligning incentives, investing in complementary nodes, and preparing for contingencies around Taiwan and other flashpoints.

US economic policy | Semiconductor industry | Supply chains | Transatlantic relations

keywords

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Wired for Resilience: Transatlantic Approaches to Semiconductor Supply Chain Security

by Barath Harithas*

Introduction

Semiconductors, the bedrock of modern economies, have vaulted from niche concern to the centre stage of economic security policy. The shortages of recent years delivered the lesson with brutal clarity. In 2021, automakers produced eight million fewer vehicles globally[1] due to chip shortages, an output loss exceeding 210 billion US dollars.[2] Average chip inventories plunged from forty days pre-pandemic to under five days in early 2022,[3] leaving industries one supply disruption away from collapse.

This fragility is unfolding amid the intensifying United States–China technology rivalry. Semiconductors have become the strategic high ground of this contest. Washington has moved decisively – blacklisting Chinese AI firms, imposing sweeping export controls on advanced chips and tools,[4] and investing 52 billion US dollars in domestic production and research and development (R&D) through

[1] Paul A. Eisenstein, "What's Ahead for the Auto Industry in 2022?", in *NBC News*, 1 January 2022, https://www.nbcnews.com/business/autos/going-change-auto-industry-2022-rcna10350.

[2] Michael Wayland, "Chip Shortage Expected to Cost Auto Industry $210 billion in Revenue in 2021", in *CNBC*, 23 September 2021, https://www.cnbc.com/2021/09/23/chip-shortage-expected-to-cost-auto-industry-210-billion-in-2021.html.

[3] US Department of Commerce, *Results from Semiconductor Supply Chain Request for Information*, 25 January 2022, https://www.commerce.gov/news/blog/2022/01/results-semiconductor-supply-chain-request-information.

[4] US Bureau of Industry and Security, *Commerce Implements New Export Controls on Advanced Computing and Semiconductor Manufacturing Items to the People's Republic of China (PRC)*, 7 October 2022, https://www.bis.doc.gov/index.php/component/docman/?task=doc_download&gid=3158.

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the CHIPS and Science Act.[5] Beijing, in turn, has doubled down on "science and technology self-reliance",[6] channelling state subsidies into fab construction and chip research.

Caught in the middle is the global semiconductor ecosystem, intricately interdependent and now geopolitically exposed. The central policy question is how can the United States and its allies de-risk and diversify without succumbing to techno-nationalist overreach?

There is a fundamental, but often overlooked, distinction that needs to be made when discussing semiconductor policy.

Each faces distinct risks:

- *Advanced chips* produced at leading-edge process nodes (5nm, 3nm and soon 2nm),[7] are indispensable for high-performance computing and AI applications. To our previous estimate, the installed base of leading-edge graphics processing units (GPUs) in the United States (such as NVIDIA's A100/H100 series) may leap from roughly 5.5 million in 2024 to 160 million by 2030.[8] Meeting this demand will require a majority of the entire wafer capacity of TSMC, the Taiwanese company that dominate semiconductor manufacture globally.[9] Access to leading-edge foundries has thus become a matter of strategic necessity. Such numbers are not mere market curiosities, they have become matters of national security concern for Washington.
- *Legacy chips*, often defined as 28nm and above[10] and less flashy, are the workhorse of industries from automotive to household appliances. Crucially, it was these older chips, not GPUs, that triggered the most acute Covid-era shortages. Demand for 40nm+ microcontrollers and analog chips overwhelmed supply, and even with fabs running at over 90 per cent utilisation, industry could not ramp up overnight.[11] The pain cascaded most visibly through the auto sector, where roughly 95 per cent of the chips in a modern car are legacy nodes.[12]

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[5] US Congress, *H.R.4346 - CHIPS and Science Act*, 9 August 2022, https://www.congress.gov/bill/117th-congress/house-bill/4346.

[6] Ardi Janjeva, Seoin Baek and Andy Sellars, "China's Quest for Semiconductor Self-Sufficiency", in *CETaS Briefing Papers*, December 2024, https://cetas.turing.ac.uk/node/303.

[7] Domenico Vicinanza, "The 'World's Most Advanced Microchip' Has Been Unveiled", in *ScienceAlert*, 7 April 2025, https://www.sciencealert.com/?p=157443.

[8] Navin Girishankar et al., "Securing Full Stack U.S. Leadership in AI", in *CSIS Commentaries*, 3 March 2025, https://www.csis.org/node/114983.

[9] Ibid.

[10] Andrew Lee, "Taking on the World's Factory: A Path to Contain China on Legacy Chips", in *FAS Policy Memos*, 6 February 2025, https://fas.org/?p=35848.

[11] US Department of Commerce, *Results from Semiconductor Supply Chain Request for Information*, cit.

[12] Rakesh Kumar, "U.S. Chip Efforts Have Focused on Advanced Semiconductors–But Low-Tech Legacy Chips Could Give China an Unexpected Edge", in *Fortune*, 18 August 2023, https://fortune.com/2023/08/18/u-s-chip-efforts-have-focused-on-advanced-semiconductors-but-low-tech-

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The semiconductor industry is thus fighting a two-front war: one over next-generation compute, the other over last-generation volume.

To date, most headlines and policy firepower have focused on the US response. But Europe remains a crucial, if underappreciated, node in this global system. The Netherlands is home to ASML, sole supplier of extreme ultraviolet (EUV) lithography machines, necessary to fabricate advanced chips.[13] Germany and France host key analog, power and automotive chip manufacturers. Europe may lack leading-edge fab capacity, but it possesses key capabilities in photonics, materials, and mid-tier production.[14]

This paper adopts a macro-to-micro lens to map the US approach to semiconductor resilience: Section 1 examines structural chokepoints in the global supply chain – who makes what, where the bottlenecks lie, and how interdependencies shape vulnerability. Section 2 provides an in-depth view of the US strategy: CHIPS Act implementation, export control enforcement, and the balancing act between onshoring and alliance-building. Section 3 explores the prospects and politics of transatlantic cooperation, from joint investments to aligned outbound investment screening regimes.

The bottom line of this paper is that securing semiconductor resilience is not a zero-sum nationalist arms race. It is a positive-sum coordination challenge. The United States and Europe must act not just in parallel but in concert – aligning incentives, investing in complementary nodes, and preparing for contingencies around Taiwan and other flashpoints.

1. Mapping the semiconductor supply chain: Advanced vs legacy chips

Resilient policymaking starts with knowing the battlefield. The semiconductor supply chain is often labelled "global," but it is not a flat, evenly distributed network. It is a concentrated one where a handful of countries and firms dominate key stages. Critically, the structure diverges sharply between two categories: (1) advanced chips (leading-edge logic and memory); and (2) legacy or mature-node chips (older-process logic, analog, power, microcontrollers, used in cars, Internet of Things devices, industrial electronics).

To understand what the United States and Europe are doing and where they must act together – we first map who holds the chokepoints.

legacy-chips-could-give-china-an-unexpected-edge.

[13] Sébastien Dauvé, "Semiconductors: Can European Industry Regain Ground?", in *Polytechnique Insights*, 2 April 2025, https://www.polytechnique-insights.com/?p=26178.

[14] Ibid.

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1.1 Design and IP: The United States' edge

At the starting line of both supply chains sits design. Here, the United States reigns supreme. US firms like Cadence and Synopsys control ~70 per cent of global electronic design automation (EDA) software,[15] the essential tools engineers use to design chips.

1.2 Fabrication: Differs by node

Fabrication, the delicate process of turning silicon wafers into working chips, reveals the starkest contrast between advanced and legacy supply chains.

a. *Advanced chips (logic and memory)* – For leading-edge logic (≤5nm), Taiwan's TSMC holds ~90 per cent of the global market for cutting-edge logic manufacturing,[16] effectively monopolising supply. For memory (dynamic random access memory/DRAM, NAND Flash),[17] Samsung (South Korea), SK Hynix (South Korea) and Micron (United States) together control most advanced memory chip production.[18] China's YMTC and CXMT have made strides but face steep technological and sanctions barriers.[19]

b. *Legacy nodes (28nm+ and analog)* – In this space, global production is distributed across a combination of contract foundries and vertically integrated firms. Among the major foundries are UMC (Taiwan), GlobalFoundries (US/Germany/Singapore) and SMIC (China).

In parallel, several leading integrated device manufacturers (IDMs) design and fabricate chips in-house. These include Infineon (Germany), STMicroelectronics (France/Italy), NXP (Netherlands) and Texas Instruments (United States). IDMs are particularly important in sectors like automotive and industrial electronics, where customisation, reliability and long product lifecycles are critical.

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[15] Zeyi Yang, "Inside the Software that Will Become the Next Battle front in US-China Chip War", in *MIT Technology Review*, 18 August 2022, https://www.technologyreview.com/2022/08/18/1058116/eda-software-us-china-chip-war.

[16] US Department of Commerce, *Biden-Harris Administration Announces Preliminary Terms with TSMC, Expanded Investment from Company to Bring World's Most Advanced Leading-Edge Technology to the U.S.*, 8 April 2024, https://www.commerce.gov/node/6670.

[17] DRAM provides high-speed, temporary working memory for active processes, while NAND Flash offers non-volatile storage, retaining data even when power is off.

[18] Jie Ye-eun, "Micron Makes Aggressive HBM Push to Challenge Samsung, SK", in *The Korea Herald*, 13 April 2025, https://www.koreaherald.com/article/10463949.

[19] Chun Byung-soo and Lee Jae-eun, "Samsung's Memory Chip Leadership at Risk as China's CXMT, YMTC Close in", in *The Chosun Daily*, 27 February 2025, https://www.chosun.com/english/industry-en/2025/02/27/6UETWICZ35AGDPJBRO46YZ3OMU.

China has rapidly expanded mature-node capacity, fuelled by state subsidies, this surge has raised alarms over potential overcapacity and price distortions.[20]

1.3 Equipment and materials: Transatlantic and allied strength

The upstream tools and materials that enable fabrication are where US, European and Japanese firms form a strong "democratic coalition".

ASML (Netherlands) is the world's sole supplier of EUV lithography, indispensable for sub-7nm manufacturing. Without ASML, there is no leading-edge production – a leverage point used in recent export controls. Even for older nodes, ASML holds ~80-90 per cent of the deep ultraviolet (DUV) lithography market,[21] alongside Nikon and Canon (Japan).[22]

Applied Materials, Lam Research, KLA (United States) and Tokyo Electron (Japan) dominate deposition, etch and metrology tools.[23] ASM International (Netherlands) leads in atomic layer deposition.[24] Japan's Shin-Etsu and SUMCO supply most silicon wafers.[25] Europe's Merck KGaA and BASF provide critical chemicals and photoresists.[26]

Ukraine's war-time neon shortages and China's gallium/germanium export restrictions exposed just how fragile some raw material dependencies remain.

1.4 Strategic takeaways

This mapping exercise reveals two broad realities: advanced supply chains are democratic-led. Cutting-edge design (United States), equipment (United States, EU, Japan), and fabrication (Taiwan, South Korea) are controlled by allies but display high geographic concentration risks.

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[20] US Bureau of Industry and Security, *Public Report on the Use of Mature-Node Semiconductors*, December 2024, https://www.bis.gov/media/documents/public-report-use-mature-node-semiconductors-december-2024.

[21] Compound & Fire, "ASML: The Semiconductor King Powering the AI Revolution", in *Deep Dives*, 3 May 2025, https://compoundandfire.substack.com/p/asml-the-semiconductor-king-powering.

[22] Ibid.

[23] Barath Harithas and Andreas Schumacher, "Where the Chips Fall: U.S. Export Controls Under the Biden Administration from 2022 to 2024", in *CSIS Commentaries*, 12 December 2024, https://www.csis.org/node/113735.

[24] Javier Correonero, "Upgrading Our Moat Rating to Wide for ASM International and BE Semiconductor", in *Morningstar Equity Research & Insights*, 29 April 2025, https://www.morningstar.co.uk/uk/news/264189/upgrading-our-moat-rating-to-wide-for-asm-international-and-be-semiconductor.aspx.

[25] Mark LaPedus, "Silicon Wafer Market: Upturn, Higher Prices", in *Semiecosystem*, 24 April 2024, https://marklapedus.substack.com/p/silicon-wafer-market-upturn-higher.

[26] The Business Research Company, "Photoresist Electronic Chemical Market Forecast 2025-2034: Growth Dynamics, Emerging Trends, and Strategic Opportunities", in *Latest Global Market Insights*, 28 April 2025, https://blog.tbrc.info/?p=185142.

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Legacy supply chains are more globally distributed but vulnerable to China's rise. Mature-node and analog chips are scattered across the United States, EU, Japan, Taiwan and China, with Beijing's subsidised overcapacity threatening to destabilise global markets.

2. The US semiconductor resilience strategy: The sword and the shield

For decades, US semiconductor strategy was laissez-faire – let market forces sort it out. Over the past two years, Washington has launched the most ambitious industrial policy effort in a generation; spending big, regulating hard, and realigning national priorities to shore up chip supply chains.

This section dissects the pillars of the US strategy: (1) *massive investment incentives* (CHIPS Act subsidies and tax credits); (2) *workforce and talent development* to incubate the next generation; (3) *export controls and tech protection* to block adversarial advances; (4) *trade enforcement tools* like tariffs and Section 301 investigations to combat non-market distortions.[27]

Throughout, one theme stands out: while the United States aims to claw back advanced logic and memory production, it is also awakening belatedly to the need to protect its legacy chip foundations.

2.1 The CHIPS Act: Big money, big bets

The centrepiece of the US resilience playbook is the CHIPS and Science Act of 2022, which commits 52.7 billion US dollars to the domestic semiconductor industry:

- 39 billion in direct manufacturing incentives,
- 13.2 billion for R&D and workforce development, and
- a 25 per cent investment tax credit for capital expenditures.[28]

This injection aims to reverse the slide in US global manufacturing share, which fell from ~37 per cent in the 1990s to ~12 per cent by 2020.[29]

[27] Section 301 investigations refer to investigations opened by the Department of Commerce under the 1974 Trade Act, which allows for the imposition of tariffs as retaliation against foreign discrimination of US companies.

[28] David Plotinsky and JiaZhen Guo, "First CHIPS for America Funding Opportunity Provides $39B for Domestic and International Semiconductor Manufacturers", in *LawFlash*, 2 March 2023, https://www.morganlewis.com/pubs/2023/03/first-chips-for-america-funding-opportunity-provides-39b-for-domestic-and-international-semiconductor-manufacturers.

[29] Semiconductor Industry Association (SIA), *SIA Applauds Enactment of CHIPS Act*, 9 August 2022, https://www.semiconductors.org/sia-applauds-enactment-of-chips-act.

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By the end of 2024, the Department of Commerce had awarded ~30.6 billion US dollars across nineteen companies, with another ~1.7 billion US dollars preliminarily proposed.

The headline recipients are the giants of semiconductor manufacturing:

- TSMC: 6.6 billion US dollars for two fabs in Arizona (4/5nm production by 2025, 3nm by 2027-28).[30]
- Intel: Up to 7.86 billion US dollars to support fabs in Ohio, Arizona and Oregon, plus advanced packaging in New Mexico.[31]
- Samsung: 4.7 billion US dollars for two Texas fabs and an R&D centre.[32]
- Micron: 6.2 billion US dollars for a DRAM megafab in New York and expansion in Idaho.[33]

Crucially, federal dollars unlock massive private and state co-investment. Intel's grant underpins a 100 billion US dollars "Ohio One" megafab;[34] Micron's New York plans involve ~40 billion US dollars over a decade, with ~5.5 billion in state incentives.[35]

This subsidy model directly tackles the cost gap between US and overseas fab construction, helping to level the playing field against subsidised competitors.

2.2 Beyond the giants: Tacking the legacy chips problem

While the United States aims to claw back advanced logic and memory production, it is also awakening belatedly to the need to protect its legacy chip foundations:

- GlobalFoundries: 1.5 billion US dollars to expand legacy-node capacity in New York and Vermont.[36]
- Texas Instruments: 1.6 billion US dollars for new analog fabs in Texas and Utah.[37]

[30] TSMC, *TSMC Arizona and U.S. Department of Commerce Announce up to $6.6 Billion in CHIPS Act Funding*, 8 April 2024, https://pr.tsmc.com/english/news/3122.

[31] US Department of Commerce, *Biden-Harris Administration Announces CHIPS Incentives Award for Intel*, 26 November 2024, https://www.commerce.gov/node/6998.

[32] National Institute of Standards and Technology (NIST) website: *Samsung Electronics (Texas)*, https://www.nist.gov/node/1855111.

[33] Jingyue Hsiao, "Micron Secures $6.165 Billion in CHIPS Act Funding to Advance U.S. Memory Manufacturing", in *Digitimes*, 11 December 2024, https://www.digitimes.com/news/a20241211VL200.

[34] Reuters, "Intel Plans $20 Billion Chip Manufacturing Site in Ohio", in *CNBC*, 21 January 2022, https://www.cnbc.com/2022/01/21/intel-plans-20-billion-chip-manufacturing-site-in-ohio.html.

[35] Micron Technology, *Micron Announces $40 Billion Investment in Leading-Edge Memory Manufacturing in the US*, 9 August 2022, https://investors.micron.com/node/43921.

[36] GlobalFoundries, *GlobalFoundries and U.S. Department of Commerce Announce Award Agreement on CHIPS Act Funding for Essential Chip Manufacturing*, 20 November 2024, https://gf.com/?p=12790.

[37] Texas Instruments, *Texas Instruments Signs Preliminary Agreement to Receive up to $1.6 Billion in CHIPS and Science Act Proposed Funding for Semiconductor Manufacturing in Texas and Utah*, 16 August 2024, https://www.ti.com/about-ti/newsroom/news-releases/2024/2024-08-16-texas-instruments-signs-preliminary-agreement-to-receive-up-to--1-6-billion-in-chips-and-science-act-proposed-funding-for-semiconductor-manufacturing-in-texas-and-utah.html.

- Wolfspeed: 750 million US dollars Funding for a silicon carbide (SiC) power chip fab in North Carolina.[38]

Significantly, the United States is also investing in packaging and assembly – historically dominated by Asia. Amkor, one of the top global players in outsourced semiconductor assembly and test (OSAT), received 407 million US dollars to build a state-of-the-art facility in Arizona.[39]

This diversified funding approach reflects a deliberate shift – the United States is not just trying to plant a few advanced fabs but to rebuild an integrated semiconductor supply chain onshore.

2.3 Export controls: Buying time by kneecapping rivals

If subsidies represent the carrot, export controls are the stick.

In October 2022, recognising the escalating computational demands of frontier AI,[40] reliant on thousands of the most advanced microprocessors and memory chips, the United States moved to weaponise its dominance over critical chokepoints[41] in the global semiconductor supply chain, which China was dependent on. It was a bold act of bureaucratic foresight – the United States had anticipated the importance of AI before ChatGPT 3.5 made it undeniable just a month later.[42]

The fact that the complex supply chains needed to produce advanced semiconductors were concentrated in the United States and a small number of allied countries further provided a singular opportunity for export control revision.

The controls targeted the sale of the following:
- Advanced semiconductors leading producers: NVIDIA, AMD, Intel, Broadcom (United States), Samsung, SK Hynix (South Korea)
- Electronic design automation (EDA) software market leaders: Synopsys,

[38] Wolfspeed, *Wolfspeed Announces $750M in Proposed Funding from U.S. CHIPS Act…*, 15 October 2024, https://www.wolfspeed.com/company/news-events/news/wolfspeed-announces-750m-in-proposed-funding-from-us-chips-act-and-additional-750m-from-investment-group-led-by-apollo-galvanizing-global-leadership-in-delivering-next-generation-silicon-carbide.

[39] Amkor Technology, *Biden-Harris Administration Announces CHIPS Incentives Award with Amkor Technology to Bring End-to-End Chip Production to the U.S.*, 20 December 2024, https://amkor.com/blog/biden-harris-administration-announces-chips-incentives-award-with-amkor-technology-to-bring-end-to-end-chip-production-to-the-u-s.

[40] Jaime Sevilla and Edu Roldán, "Training Compute of Frontier AI Models Grows by 4.5x per Year", in *Epoch AI*, 28 May 2024, https://epoch.ai/blog/training-compute-of-frontier-ai-models-grows-by-4-5x-per-year.

[41] Saif M. Khan, "Securing Semiconductor Supply Chains", in *CSET Policy Briefs*, January 2021, https://cset.georgetown.edu/publication/securing-semiconductor-supply-chains.

[42] Bernard Marr, "A Short History of ChatGPT: How We Got to Where We Are Today", in *Forbes*, 19 May 2023, https://www.forbes.com/sites/bernardmarr/2023/05/19/a-short-history-of-chatgpt-how-we-got-to-where-we-are-today.

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Cadence (United States), Siemens EDA (Germany/United States)
- Semiconductor manufacturing equipment lithography: ASML (Netherlands), Tokyo Electron (Japan), Process Tools: Lam Research, Applied Materials (United States)
- Critical components needed to develop machinery metrology/inspection: KLA Corporation (United States), Light Sources: Cymer (United States)[43]

The United States operated with transitive precision. First, it blocked direct access to the advanced semiconductors needed for frontier AI development. Then, it denied Beijing the tools the software and machinery needed to design and fabricate the chips themselves. Finally, it pre-empted any efforts to indigenise by obstructing access to the critical components required to build the machinery domestically. The cascading sequence of restrictions aimed to trap China in a technological cul-de-sac and sustain the United States' dominance.[44]

Crucially, the United States secured alignment from key allies:
- The Netherlands expanded controls to cover advanced DUV lithography, alongside its long-standing EUV export bans.
- Japan imposed controls on etching, deposition, and cleaning tools.

2.4 Trade enforcement: Tariffs and Section 232/301 hammer

In late 2024, Washington escalated its toolkit by launching a Section 301 investigation[45] into China's industrial policies, particularly targeting mature-node semiconductors. The probe, authorised under the same statute that fuelled the first Trump-era trade war, targets Beijing's extensive subsidies and non-market practices. If confirmed, the investigation could result in:
- tariffs on Chinese semiconductor imports;
- restrictions on US firms sourcing certain Chinese legacy chips; or
- negotiated agreements to moderate Chinese overproduction.

The strategic aim is to prevent a repeat of the solar panel or steel overcapacity crisis, where Chinese state-subsidised surpluses drove Western competitors out of business.

2.5 Gaps, risks and the Trump factor

Despite its ambition, the US semiconductor strategy faces three glaring risks:
1. Funding sustainability: The CHIPS Act is a one-off, front-loaded package. Operating support, follow-on R&D funding ("CHIPS 2.0"), and ecosystem

[43] Barath Harithas and Andreas Schumacher, "Where the Chips Fall", cit.

[44] Ibid.

[45] US Trade Representative (USTR), *USTR Initiates Section 301 Investigation of China's Acts, Policies, and Practices Related to Targeting of the Semiconductor Industry for Dominance*, 23 December 2024, https://ustr.gov/node/13974.

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resilience (e.g., substrates, advanced packaging) may need additional waves of investment. Political appetite for further subsidies remains uncertain, especially in a more fiscally hawkish environment.

2. Political uncertainty: President Donald Trump has signalled scepticism toward the CHIPS Act, calling it "government picking winners and losers". He might scale back subsidies, impose new conditions or prioritise tariffs over allied cooperation. Moreover, Trump-era tensions with Europe – over auto tariffs, defence spending, and trade balances – could disrupt delicate transatlantic semiconductor alignments.
3. Overcapacity and geopolitical timing: If the global fab buildout outpaces demand (especially in cyclical sectors like memory), the result could be a self-inflicted glut. And crucially, even with aggressive reshoring, the United States will remain reliant on Taiwan's TSMC through the late 2020s. A Taiwan contingency would imperil global advanced chip supply before US domestic fabs come fully online.

3. Transatlantic semiconductor cooperation: What's realistic, what's necessary

It is easy to wax lyrical about "transatlantic partnership" in semiconductors. After all, the United States and Europe share democratic values, advanced industrial bases and deep economic ties. But the reality is harder. Both sides have differing industrial traditions, their own domestic pressures, and (especially under a second Trump Administration) increasingly transactional instincts.

This section cuts through the niceties to ask: what kinds of US–EU semiconductor cooperation is realistically feasible, even under political strain? Which ideas are merely diplomatic window dressing, and which can actually deliver meaningful resilience benefits?

A pragmatic, layered approach is essential: focus on quiet, technocratic cooperation below the political surface; leverage areas of unique mutual dependency (where neither side can go it alone); and target a few novel mechanisms that do not depend on fragile political goodwill. Semiconductor resilience, after all, is not a diplomatic talking point, it is an operational necessity.

3.1 Aligning incentives without fighting over the same fabs

Both the United States and EU have launched bold industrial strategies – the CHIPS Act and the European Chips Act – each aiming to rebuild domestic semiconductor capacity. But without coordination, they risk competing for the same handful of global players (TSMC, Intel, Samsung) or over-incentivising the same segments while leaving others neglected.

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To address this, the United States and EU created a subsidy transparency mechanism under the Trade and Technology Council (TTC) to share details on grant programmes and capacity expansion plans. This is a good start, but the TTC is politically fragile and may not survive the Trump factor or broader US–EU tensions.

A practical fallback is for agencies like the US Department of Commerce and the European Commission to establish a quiet, staff-level coordination channel that persists even if the TTC falters. This could involve informal "gentlemen's agreements" to avoid bidding wars – e.g., the EU focuses subsidies on mature-node, automotive and power chips (its core strengths), while the United States leans into leading-edge logic, memory and advanced packaging. This soft division of labour is already emerging in practice: Europe's 10 billion euro support package for Intel's Magdeburg fabs and its projects with STMicroelectronics and Infineon tilt toward European industrial niches, while the United States bets big on Arizona, Ohio and Texas for bleeding-edge fabs.

It is unrealistic to expect perfectly harmonised subsidy strategies – both sides will pursue national interests – but targeted transparency to avoid wasteful duplication is politically feasible and economically wise.

3.2 Keeping the export controls front aligned

One of the clearest US–EU successes so far has been their alignment on export controls targeting China's access to advanced semiconductor tools and equipment. The Dutch (with ASML) and the Japanese came on board after extensive US diplomatic pressure in 2023.[46]

But as the United States ratchets up its rules, tightening thresholds for AI chip performance, closing loopholes, or adding new controlled technologies – it will need EU alignment.

The most feasible way forward here is continued task force coordination at the technocratic level – not grand political gestures. US and EU officials should:

- share advance notice of planned export rule changes;
- conduct joint technical assessments of which tools, components or software to cover; and
- coordinate enforcement intelligence (for example, tracking suspicious export routes or front companies).

This does not require a new formal treaty or expanded TTC mandate. It requires well-staffed, well-resourced regulatory teams with routine, confidential backchannel communication – something that can survive political turbulence, even under a more unilateralist US Administration.

[46] Barath Harithas and Andreas Schumacher, "Where the Chips Fall", cit.

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3.3 Crisis coordination: Early warning, not empty summits

Russia's invasion of Ukraine, China's export restrictions on gallium and germanium and fears over Taiwan prompted the United States and EU to establish a joint early warning mechanism for semiconductor disruptions.

This is one of the most pragmatic and feasible cooperation areas: it is purely operational, benefits both sides, and is largely insulated from high-level political drama.

The United States and EU should:

- expand it to include like-minded partners – Japan, South Korea, Taiwan, and possibly the United Kingdom – creating a global semiconductor alert network;
- develop pre-agreed crisis protocols, such as coordinated release of stockpiles, surge production plans or reciprocal fallback supply arrangements.

It is unrealistic to expect full-blown "allied allocation plans" for something like a Taiwan crisis (where geopolitics would overwhelm bureaucratic plans), but even lightweight contingency playbooks can reduce chaos in moments of acute supply shock.

3.4 Joint R&D and standards: Quiet wins, not grandiose pledges

Joint US–EU research programmes are often promised in high-level communiqués but deliver little without concrete funding and institutional mechanisms.

Here, a practical and novel step would be to launch:

- A Transatlantic semiconductor research fund: Even a modest 100–200 million US dollars co-funded programme (matching US and EU money) that supports joint university-industry projects in areas like post-silicon materials, advanced packaging, or low-energy computing. The Horizon Europe programme could link to US National Science Foundation calls, using joint evaluation panels and shared IP frameworks.
- A standards cooperation initiative: Focused not on broad political statements but on niche, actionable domains – e.g., hardware-based security standards, chip traceability protocols, or green manufacturing benchmarks. Agencies like the US National Institute for Science and Technology and the European Telecommunications Standards Institute and European Committee for Electrotechnical Standardisation can work together to harmonise standards, giving Western firms a head start and indirectly setting global norms.

These efforts are low political cost and high resilience payoff, especially if framed as technical collaborations, not geopolitical grandstanding.

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3.5 Co-investment mechanisms: A semiconductor venture fund

One genuinely underexplored idea is a US–EU joint semiconductor venture fund targeting startups developing critical supply chain technologies:

- lithography alternatives (beyond EUV);
- AI-driven EDA tools;
- novel semiconductor materials (beyond silicon, GaN, SiC);
- advanced packaging solutions.

By co-investing, the United States and EU can reduce reliance on Chinese capital, share intellectual property, and ensure dual-location development and where both sides co-fund and co-own technology breakthroughs.

This would require modest initial capital (hundreds of millions, not tens of billions) but would have a disproportionately large symbolic and strategic impact, signalling deep transatlantic tech alignment.

3.6 Practical recommendations

Given these realities, US–EU semiconductor cooperation should focus on:

- *institutional durability*: Embed coordination mechanisms in regulatory agencies and industrial bodies, not just high-level councils.
- *technocratic quiet channels*: Keep lines open at the working level, even if political leaders clash.
- *low-cost, high-impact initiatives*: Prioritise early warning systems, joint R&D funds, co-investment vehicles, and standards alignment over sweeping new treaties.
- *mutual fallback mechanisms*: Quietly prepare reciprocal support plans for severe supply disruptions.

4. Conclusion: A resilience architecture for an uncertain era

The return of Trump to the White House has already upended many assumptions in US–EU relations. The TTC, once envisioned as a flagship mechanism for transatlantic coordination, now teeters under the weight of an "America First" doctrine sceptical of formal alliances and multilateral structures. Yet, the cold reality of the semiconductor supply chain imposes constraints that even political shifts cannot fully override.

No matter the rhetoric from Washington or Brussels, the fact remains: the United States and Europe are bound together in this domain by necessity, not sentiment. The United States needs ASML's lithography and Europe, for its part, needs US chip design, equipment and critically the diplomatic muscle to sustain a coordinated export control regime on China.

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The challenge ahead is clear. Policymakers on both sides of the Atlantic must now shift from headline-grabbing pledges to pragmatic, institutionalised cooperation that can endure even under strained political conditions. That means embedding early warning mechanisms, coordinating industrial incentives, and aligning export control updates at the agency level – quiet, operational work that does not require top-level political harmony to succeed. It also means embracing a transactional framing when necessary – cooperation not as a diplomatic favour, but as a mutual economic and security imperative.

The Trump Administration's scepticism toward multilateralism may complicate this work, but it does not erase its necessity. Indeed, the irony is that the more transactional and volatile global politics becomes, the more valuable and stabilizing these technical, bottom-up cooperation mechanisms will be.

In short, the United States and Europe are now in the business of rewiring the global semiconductor circuit for security and durability. It will not be elegant, it will not be smooth, but it is, unmistakably, the work of this geopolitical moment.

Updated 12 June 2025

List of acronyms

ASML	Advanced semiconductor materials lithography
CXMT	ChangXin Memory Technologies
DRAM	Dynamic random access memory
DUV	Deep ultraviolet
EDA	Electronic design automation
EU	European Union
EUV	Extreme ultraviolet
GaN	Gallium nitride
GPU	Graphics processing unit
IDM	Integrated device manufacturer
nm	Nanometre
OSAT	Outsourced semiconductor assembly and test
R&D	Research and development
SiC	Silicon carbide
SMIC	Semiconductor Manufacturing International Corporation
SUMCO	Silicon United Manufacturing Corporation
TMSC	Taiwan Semiconductor Manufacturing Company
TTC	Trade and Technology Council
UMC	United Microelectronics Corporation
US	United States
YMTC	Yangtze Memory Technology Co.

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